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UTILITY PATENT APPLICATION TRANSMITTAL

(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
1920/107Total Pages in this Submission
30**TO THE ASSISTANT COMMISSIONER FOR PATENTS**Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

SEMICONDUCTOR PACKAGING

and invented by:

Behnam Tabrizi

If a **CONTINUATION APPLICATION**, check appropriate box and supply the requisite information:☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____

Which is a:

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☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____

Enclosed are:

Application Elements

1. ☐ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 17 pages and including the following:
 - a. ☒ Descriptive Title of the Invention
 - b. ☒ Cross References to Related Applications (if applicable)
 - c. ☐ Statement Regarding Federally-sponsored Research/Development (if applicable)
 - d. ☐ Reference to Microfiche Appendix (if applicable)
 - e. ☒ Background of the Invention
 - f. ☒ Brief Summary of the Invention
 - g. ☒ Brief Description of the Drawings (if drawings filed)
 - h. ☒ Detailed Description
 - i. ☒ Claim(s) as Classified Below
 - j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*

- a. ☐ Formal Number of Sheets _____
b. ☒ Informal Number of Sheets 5

4. ☒ Oath or Declaration

- a. ☐ Newly executed *(original or copy)* ☒ Unexecuted
b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
c. ☒ With Power of Attorney ☐ Without Power of Attorney
d. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application,
see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*

The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche *(Appendix)*

7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*

- a. ☐ Paper Copy
b. ☐ Computer Readable Copy *(identical to computer copy)*
c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*

9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Acknowledgment postcard

14. ☒ Certificate of Mailing

☐ First Class ☒ Express Mail *(Specify Label No.):* EL543499264US

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

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Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. ☐ Additional Enclosures (please identify below):

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	39	- 20 =	19	x \$18.00	\$342.00
Indep. Claims	8	- 3 =	5	x \$80.00	\$400.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
BASIC FEE					\$710.00
OTHER FEE (specify purpose)					\$0.00
TOTAL FILING FEE					\$1,452.00

- ☐ A check in the amount of _____ to cover the filing fee is enclosed.
- ☐ The Commissioner is hereby authorized to charge and credit Deposit Account No. _____ as described below. A duplicate copy of this sheet is enclosed.
- ☐ Charge the amount of _____ as filing fee.
 - ☐ Credit any overpayment.
 - ☐ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
 - ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).


Signature

John J. Stickevers
Registration No. 39,387
BROMBERG & SUNSTEIN LLP
125 Summer Street
Boston, MA 02110
(617) 443-9292

Dated: October 2, 2000

cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application for
Semiconductor Packaging

Invention of: Behnam Tabrizi
153 Collins Drive
Marlborough, MA 01752

Attorney docket number:
1920/107

Attorneys:
Bromberg & Sunstein LLP
125 Summer Street
Boston, MA 02110-1618
Tel: (617) 443-9292
Fax: (617) 443-0004



09/29/00

Semiconductor Packaging

Priority

This application claims priority from United States provisional patent
5 application serial number 60/156,739, filed September 30, 1999, entitled "Semiconductor
Packaging", the disclosure of which is incorporated herein by reference.

Technical Field

The present invention relates to electronic devices and more particularly to
packaging for electronic devices.

Background Art

Semiconductor electronic devices often include a package surrounding the device
to permit handling and electrical connections while providing protection for the
electronic device from external environmental influences. Packages are typically
manufactured out of plastic, metal, ceramic or glass.

Summary of the Invention

In accordance with one aspect of the invention, an electronic component and a
method for making an electronic component are disclosed. The electronic component
has a silicon package. The silicon package has a recess formed thereon in which a
conductive region is placed. A bare die electronic device is disposed in the recess. The
20 device has a top, a bottom, sides and a plurality of terminals, including a non-top
terminal. The non-top terminal is electrically coupled to the conductive region. The
electronic component is constructed by first creating a recess in a silicon wafer to a
depth substantially equal to the first dimension of the bare die electronic device. A
conductive material is applied to the recess. The electronic device is inserted into the
25 recess so that the bottom terminal is coupled to the conductive material. A dielectric or
other planarizing material is applied into the recess. Top and bottom contacts are then
applied to form the electronic component so that it may be used as a ball grid array

(BGA) package. The top contact is electrically coupled to the top terminal of the electronic device and the bottom contact is coupled electrically to the conductive material.

In another embodiment, multiple recesses are created on a single silicon wafer and electronic devices are each inserted into one of the multiple recesses. The silicon wafer may then be cut to form multiple electronic components. Prior to the step of cutting, each of the electronic components may be tested.

In another embodiment where the electronic component is a chip device, one of the terminals of the device is a top contact located on the top of the device and the package has a top in which the recess is located. The top of the package also includes a contact coupled electrically via the conductive region to the non-top terminal.

Brief Description of the Drawings

The foregoing features of the invention will be more readily understood by reference to the following detailed description taken with the accompanying drawings in which:

Fig. 1 is a side view of one embodiment of the invention in which an electronic device resides within a silicon package.

Fig. 2 is a flow chart of the steps used in creating a silicon package that is a Ball Grid Array (BGA) and that is also a Wafer Level Chip-Scale Package (WLCSP).

Fig. 3 is a side view of a silicon wafer having multiple electronic devices.

Fig. 4 shows a top view of a silicon wafer that has multiple cavities that are etched into the silicon, each cavity for receiving an electronic device to form multiple packages.

Fig. 5 is a side view of a planar electronic device positioned within a package with the terminals of the electronic device redistributed.

Detailed Description of Specific Embodiments

Fig. 1 is a side view of an electronic component. The electronic component is formed by a silicon package 10 from a silicon wafer surrounding an electronic device 12, preferably a bare die semiconductor device. The silicon package 10 includes a recess 14 in which the electronic device 12 resides. The electronic device 12 in the embodiment shown is a two-terminal device, although other multi-terminal devices, including both vertical and planar devices, may be used. The electronic device shown is a vertical device having a top terminal 15 and a bottom terminal 16. In the recess of the package, a conductive region 17 exists. The conductive region 17 covers all or a portion of the recess 14 and extends to a portion of the top 18 of the silicon package 10. The bottom terminal 16 of the two-terminal electronic device is electrically coupled to the conductive region 17. In preferred embodiments the conductive region is formed from metals such as titanium, copper and chrome. The bottom terminal 16 of the electronic device is secured to the conductive region by a conductive epoxy or solder 19. The recess 14 is filled with dielectric material 20 that surrounds the electronic device 12. If the dielectric layer 20 covers the top terminal 15 of the electronic device 12, the dielectric 20 that resides above the top terminal 15 is removed through photolithography. Dielectric may also be removed at a point where a solder contact for the bottom terminal is desired. A metalization layer 22 is applied over the dielectric after the top terminal 15 of the electronic device 12 is exposed. The metalization is deposited and patterned by standard methods to the desired routing including solder contact areas. In the shown embodiment, another layer of dielectric 25 resides on top of the metalization layer 22 fully encasing the electronic device 12 and only leaving the contacts exposed. It should be understood by those of ordinary skill in the art that for certain electronic devices a second layer of dielectric may not be needed. The solder contacts 21 are then created and preferably reside in the same plane so that the completed electronic component may be easily flip mounted onto a circuit board. In the preferred embodiment, the electronic device is a diode. However, it should be

understood to one of ordinary skill in the art that other semiconductor devices, integrated circuits, or other electronic devices may be placed within the silicon package. This process produces a Wafer Level Chip-Scale Package (WLCSP) using silicon as the package.

5 The solder contacts for the terminals of the electronic device reside on the same side of the package allowing for surface mount assembly operation similar to a Ball Grid Array (BGA) package. It should be understood by those skilled in the art that other package materials may be used for creating a WLCSP instead of silicon. These other package materials must be sufficiently rigid to prevent breakage or exposure of
10 the bare die. Further, the package material should be capable of being metalized, and should be capable of having a portion of the material removed so as to create a cavity or a recess.

In Fig. 2 is shown a flowchart of the steps for packaging a bare die electronic device creating an electronic component. The method as described uses a standard
15 silicon wafer to create one or more packages. The silicon wafer may be processed with most of the same tooling as used for wafer level device creation. In the preferred embodiment a silicon package creates a WLCSP. A recess is formed in a silicon wafer by either etching or sawing a trench in the wafer (200). The etching process could be dry etching or chemical wet etching which is known to those skilled in the art. The
20 chemical etching step is normally performed by using Si_3N_4 as mask on the top surface of the silicon wafer. The mask is patterned to the desired cavity size(s) and location(s). The cavity etch is an anisotropical etch using a solution of KOH and treta-methyl ammonium hydroxide. The cavities created by this process will typically have sloped side walls of about 54 degrees. The recess is created so that an electronic device may
25 reside within the recess. The depth of the recess is approximately the thickness of the electronic device. To the recess is applied at least one layers of conductive material (210). In case of devices with small contacts (approximately .003 inches in diameter or

less), it is preferred that a layer of a dielectric such as bisbenzocyclobutene (BCB) is deposited on top of the electronic device covering the entire top surface except for contact terminals and saw / scribe borders separation for device clearance (Fig. 3). In the preferred embodiment, the conductive material is applied in three layers. The first layer is titanium followed by a layer of copper and a layer of chrome, which cover the contour of the recess and at least a portion of the top of the silicon wafer. A layer of electrically conductive epoxy or solder is placed in the recess to assure that the device is mechanically secured and the electric device is electrically coupled to the conductive material for devices with non-top terminals. The electronic device is placed within the recess of the silicon wafer so that the bottom of the electronic device comes into contact with the conductive material within the recess (220). Silver epoxy is then cured or the solder is reflowed, attaching the device to the bottom of the recess. Next, a layer of dielectric, such as BCB, is placed into the recess (230). Enough dielectric is added to fill the recess so that the recess is approximately planarized. The cavity fill process is done by covering a preheated silicon wafer (to reduce the viscosity of the BCB) and driving the BCB dielectric into the cavities and removing the excess material using a roller and blade drawn across the wafer. If needed another layer of dielectric can be spun on to achieve the desired planarization. The dielectric layer completely covers the electronic device, but it is desirable to keep the top terminal of the electronic device exposed. Dielectric must be subsequently removed from the top terminal and also an area on the top surface of the silicon wafer adjacent to the recess allowing direct exposure to the conductive material. One method of achieving this is by masking and removing the dry-etch BCB from the top terminal of the electronic device and desired area on the top surface of the silicon wafer. In an alternative method, a sufficient amount of the dielectric material is removed to expose the entire top surface of the silicon wafer and the top terminal of the electric device. Next, a layer of photo definable BCB is deposited and defined exposing the desired contact areas. A patterned metalization layer is

applied to the top of the dielectric and the exposed surface. A last layer of dielectric is added for further insulation so that the only exposed conductive elements are the contacts for the top and bottom terminals. Solder is then deposited onto the exposed conductive elements, forming solder contacts in the appropriate positions such that an electronic coupling occurs between the solder contact and the top (240) and bottom terminals (250) of the device. This process does not require wire/tab bonding nor does it need a flip-chip to create this wafer level BGA CSP.

The method may be implemented on a silicon wafer of adequate depth for holding an electronic device. Multiple cavities may be formed for creating multiple packages on the same silicon wafer as shown in Fig.4. The silicon wafer may be etched to create cavities or sawn to create trenches that are spaced to allow for the silicon wafer to be cut so that individual packaged electronic components may be produced. In Fig. 4 a 4 x 4 array of cavities is shown on a silicon wafer. Wafer probing of the electronic components may be accomplished prior to the sawing process for separating the completed electronic components.

In an alternative embodiment, multiple-die electronic components may be packaged by using the above-described technique. A silicon wafer having multiple cavities is formed where the cavities have different dimensions to accommodate different bare die electronic devices. The various bare die electronic devices are placed into their respectively dimensioned cavities and processed as before to create individual Chip-CSP's wherein each chip has metalized contacts. By creating contacts for each device, an additional layer of metalization may be applied which electrically couples the multiple electronic devices. A further layer of dielectric may be applied and solder contacts placed in appropriate positions. Separation of the completed multiple-die electronic components may occur by sawing the package. By creating additional cavities in a silicon wafer, multiple multiple-die electronic components may be created from a single silicon wafer.

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In Fig. 5 is shown a package 510 for a bare die planar electronic device 520 that has all terminals 540 on one side of the chip. In this embodiment, the terminals 540 of the device 520 are repositioned using the technique above. The bare die 520 is placed into a recess 515 of the package 510 and is adhered to the package using an adhesive 530 to mechanically couple the bare die 520 and the package 510. Into the portion of the recess 515 that is not filled by the bare die is placed a planarizing dielectric material 550. The planarizing material 550 creates an essentially planar surface for applying a layer of metalization 560 so that the terminals 540 of the bare die 520 may be repositioned. Once the terminals 540 are repositioned, a second layer of dielectric 570 is applied keeping only the positions of the final contacts exposed. At the desired position of the final contact a metal contact 580 or soldering bump is added. The electronic component 500 is electrically exposed only at the repositioned contact points 580 with the rest of the electronic device 520 shielded from electrical coupling by the package 510 or dielectric 570. In such a fashion, planar electronic devices having terminals that are positioned too close together and are at such a small scale that the terminals cannot maintain their electrical independence when placed on a circuit board may be made effectively larger by repositioning the contacts on the top of the package. Similarly, the terminals can be repositioned in any configuration that is more convenient for the end user of the electronic components. Thus, utilizing wafer-level processing, a smaller device may be made to be compatible with the dimensional requirements of a circuit board for fabrication of a more complicated product or subassembly.

In another embodiment, non-silicon based semiconductor bare die electronic devices , for example Gallium Arsenide electronic devices, may be made into Chip-CSPs by applying the process described above.placing.

25 In another embodiment, passive elements such as resistors, capacitors, and inductors may be added on a redistribution layer or on the additional dielectric layers to provide a higher-level integrated electronic component.

What is claimed is:

1 An electronic component comprising:
a silicon package having a recess, the recess including a conductive region; and
a bare die electronic device having a top, a bottom, sides, and a plurality of
5 terminals, including a non-top terminal, the device being disposed in the recess, and
wherein the non-top terminal is electrically coupled to the conductive region.

2. An electronic component according to claim 1, wherein:
the conductive region is formed by metalization.

3. An electronic component according to claim 2, wherein:
the metalization is achieved through a deposition process.

4. An electronic component according to claim 1, wherein the conductive region
comprises:
a first layer of titanium;
a second layer of copper deposited on the first layer; and
a third layer of chrome deposited on the second layer.

5. An electronic component according to claim 1, wherein:
the device is physically coupled to the package by the conductive region.

6. An electronic component according to claim 1, further comprising:
a dielectric that is deposited so as to at least partially fill the recess.

7. An electronic component according to claim 1, further comprising:

a plurality of metalized bumps in a plane, wherein each terminal is electrically coupled to at least one bump, and each bump is electrically coupled to at most one electrically distinct terminal.

5 8. An electronic component according to claim 7, wherein:

the package includes a top and a bottom; and

the bumps are located above the top of the package.

9. An electronic component according to claim 1, wherein:

10 The device is a vertical device and the bottom of the device is coupled to the package in the recess.

10. An electronic component according to claim 1, further comprising:

15 a second conductive region coupled to a terminal other than the non-top terminal.

11. An electronic component according to claim 1, further comprising:

20 a plurality of contact including at least a first contact and a second contact, the first contact being electrically coupled to the non-top terminal and the second contact being electrically coupled to a terminal other than the non-top terminal.

12. An electronic component according to claim 11, wherein:

the plurality of contacts reside in the same plane.

25 13. An electronic component according to claim 11, further comprising:

a second layer of dielectric completely covering the silicon package and the device except for the plurality of contacts.

14. An electronic component comprising:

a package having a recess, the recess including a first deposition-processed conductive region; and

a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal and a top terminal, the device being disposed in the recess, wherein the non-top terminal is electrically coupled to the conductive region and the top terminal is mechanically coupled to a second deposition-processed conductive region wherein at least a portion of the first and second conductive regions are essentially planar.

15. An electronic component according to claim 14, wherein:
the second conductive region is a solder bump.

16. An electronic component comprising:

a silicon package having a recess, the recess including a conductive region; and
an electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal located in a region other than the top of the device, the device being disposed in the recess, wherein the non-top terminal is electrically coupled to the conductive region.

17. An electronic component according to claim 16, wherein:

one of the terminals of the device is a top contact located at the top of the device;
and

the package has a package top, wherein the package top also includes a contact coupled electrically via the conductive region to the non-top terminal.

18. A component according to claim 16, wherein:

the conductive region comprises a layer of metal; and
the electronic device resides within the recess and the metal is electrically
coupled to the bottom terminal of the device.

5 19. An electronic component according to claim 18, further comprising:
a layer of insulation coupling the silicon package to the electronic device.

20. An electronic component according to claim 18, wherein the metal of the
conductive region extends to a portion of the package top, the electronic
10 component further comprising:
a bottom contact electrically coupled to the metal on the package top.

21. An electronic component comprising:
an electronic device having a first terminal and a second terminal, wherein a first
15 dimension is defined therebetween;

a silicon package having a first surface and a second surface, the silicon package
having a recess on the first surface that has a depth that is substantially equal to the first
dimension, the silicon package further having a layer of metal applied to the recess and
a to a portion of the first surface, wherein the electronic device resides within the recess
20 and the second terminal is coupled to the metal; and

a layer of insulation coupling the electronic device to the silicon package.

22. An electronic component according to claim 21, further comprising:

a first contact coupled to the first terminal; and

25 a second contact coupled to the metal residing on the first surface of the silicon
package.

23. A method of packaging an electronic device to create an electronic component, the electronic device having a top terminal and a bottom terminal, a first dimension being defined by the distance between the top terminal and the bottom terminal, the method comprising:

5 creating a recess in a silicon wafer, the recess having a depth substantially equal to the first dimension of the electronic device;

applying a conductive material to the recess;

inserting the electronic device into the recess so that the bottom terminal is coupled to the conductive material;

10 applyin a dielectric into the recess;

applying a top contact electrically coupled to the top terminal of the electronic device; and

applying a bottom contact electrically coupled to the conductive material.

15 24. An electronic component according to claim 23, wherein the step of applying the conductive material comprises:

applying a first layer of titanium;

applying a second layer of copper on the first layer; and

applying a third layer of chrome on the second layer.

20 25. An electronic component according to claim 23, wherein the step of applying the dielectric into the recess comprises:

applying a dry etch bisbenzocyclobutene dielectric;

removing the dry etch bisbenzocyclobutene dielectric from the top terminal and

25 a part of the conductive layer;

applying a photo defineable bisbenzocyclobutene dielectric; and

exposing the top terminal and the part of the conductive layer.

26. The method according to claim 23, wherein:

the silicon wafer has a top and a bottom, the recess being created on a portion of
the top, and wherein the bottom contact is located on the top of the silicon wafer to
enable surface mounting.

27. The method according to claim 26, wherein multiple recesses are created on a
single silicon wafer and electronic devices are each inserted into one of the
multiple recesses.

28. The method according to claim 27, wherein at least one of the electronic devices
is a resistor, diode, capacitor, or inductor.

29. The method according to claim 27, the method further comprising:
cutting the silicon wafer to form multiple electronic components.

30. The method according to claim 29, further comprising:
prior to the step of cutting, testing each of the electronic components.

31. The method according to claim 23, wherein:
the electronic component is a ball grid array packaged component.

32. An electronic component comprising:
a non-molded package having a package top and a recess;
a planar bare die electronic device having a top, a bottom, sides, and a plurality
of contacts, the device being disposed in the recess; and

a planarizing material filling the recess not occupied by the device to substantially create a level plane that includes the top of the device.

33. An electronic component according to claim 32, wherein:

5 the package is silicon.

34. An electronic component according to claim 32, further comprising:
a metalization layer.

10 35. An electronic component according to claim 34, wherein:
the metalization layer couples each contact to a redistribution point on the package top, and each contact remains electrically distinct.

36. An electronic component according to claim 35, further comprising:
15 a plurality of conductive bumps, each bump being disposed at a redistribution point.

20 37. A method of packaging an electronic device to create an electronic component,
the electronic device having a top surface and a plurality of terminals located at the top surface, the method comprising:
providing a package having a recess, the recess having a contour;
disposing the device within the recess;
mechanically coupling the device to a surface following the contour of the recess;
filling a portion of the recess not occupied by the device with a planarizing
25 material to substantially create a level plane, wherein the plane includes the top surface of the device;
creating a plurality of redistribution points on the level plane; and

electrically coupling each of the plurality of terminals with at least one redistribution point.

38. A method of packaging an electronic device to create an electronic component, the device having a device top and a plurality of terminals including a first terminal located at the device top and a second terminal located at a region other than the device top, the first and second terminals being separated by a distance defining a first dimension, the method comprising:

providing a package with a surface and a recess, the recess having a contour, wherein at least a portion of the contour extends from the surface to a depth substantially equal to the first dimension;

applying a layer of electrically conductive material to at least a portion of a surface following the contour of the recess;

disposing the device within the recess so that the second terminal is coupled to the electrically conductive region and at least a portion of the device top is substantially in the same plane as the surface of the package;

applying a first electrically conductive bump that is coupled to the first terminal; and

applying a second electrically conductive bump on the surface of the package, the bump being coupled to the electrically conductive material.

39. An electronic component according to claim 38, wherein the step of applying the layer of electrically conductive material comprises:

applying a first layer of titanium;

applying a second layer of copper on the first layer; and

applying a third layer of chrome on the second layer.

Semiconductor Packaging

Abstract

An electronic component and a method for making an electronic component are disclosed. The electronic component has a silicon package. The silicon package has a recess formed thereon in which a conductive region is placed. A bare die electronic device is disposed in the recess. The device has a top, a bottom, sides and a plurality of terminals, including a non-top terminal. The non-top terminal is electrically coupled to the conductive region. The electronic component is constructed by first creating a recess in a silicon wafer to a depth substantially equal to the first dimension of the bare die electronic device. A conductive material is applied to the recess. The electronic device is inserted into the recess so that the bottom terminal is coupled to the conductive material. A dielectric or other planarizing material is applied into the recess. Top and bottom contacts are then applied to form the electronic component so that it may be used as a ball grid array package. The top contact is electrically coupled to the top terminal of the electronic device and the bottom contact is coupled electrically to the conductive material.

[131086]

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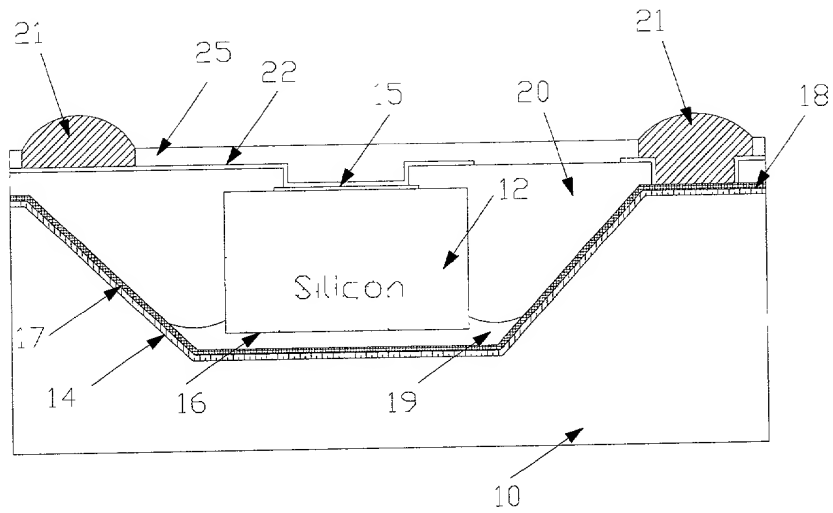


Figure - 1

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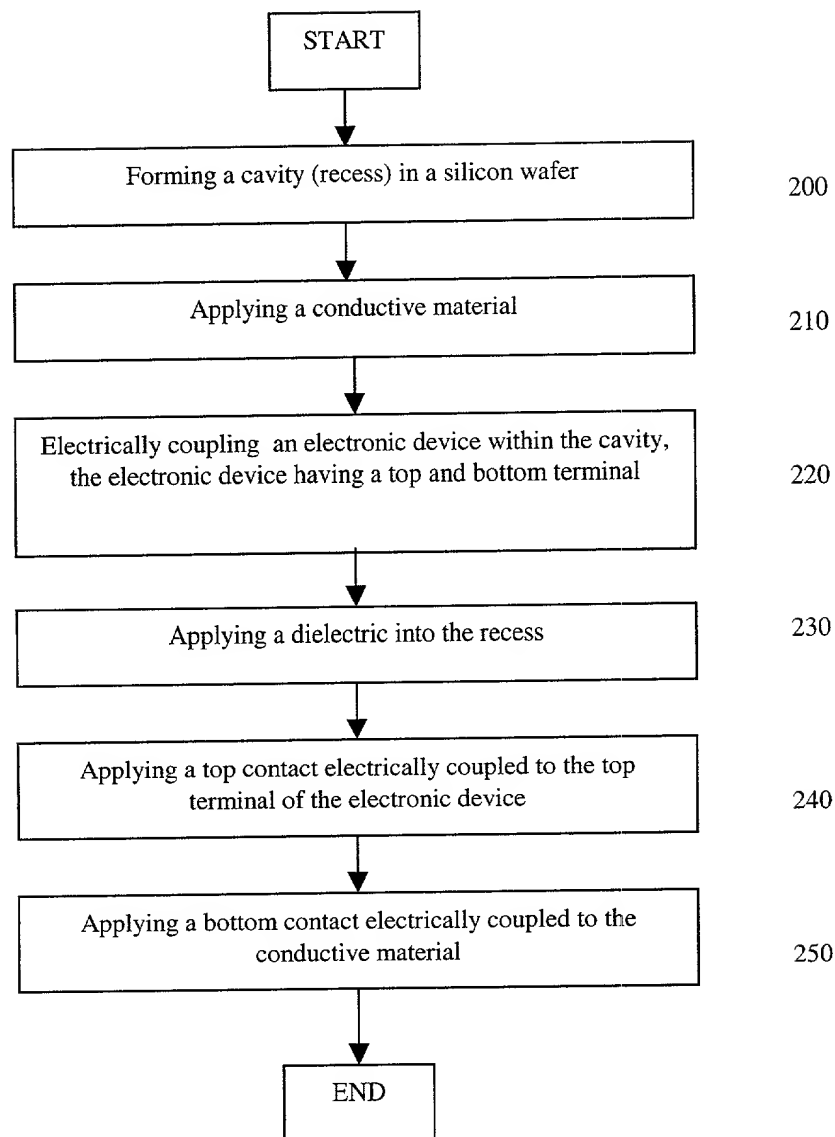


Figure - 2

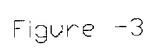


Figure-4

Docket No.
1920/107

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR PACKAGING

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____ and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Priority Not Claimed

(Number)

(Country)

(Day/Month/Year Filed)

☐

(Number)

(Country)

(Day/Month/Year Filed)

☐

(Number)

(Country)

(Day/Month/Year Filed)

☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

60/156,739

September 30, 1999

(Application Serial No.)

(Filing Date)

(Application Serial No.)

(Filing Date)

(Application Serial No.)

(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)

(Filing Date)

(Status)
(patented, pending, abandoned)

(Application Serial No.)

(Filing Date)

(Status)
(patented, pending, abandoned)

(Application Serial No.)

(Filing Date)

(Status)
(patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

Bruce D. Sunstein	27,234	Elizabeth P. Morano	42,904
Timothy M. Murphy	33,198	Sonia K. Guterman	44,729
Robert M. Asher	30,445	Keith J. Wood	45,235
Samuel J. Petuchowski	37,910	Karen A. Buchanan	37,790
Harriet M. Strimpel	37,008	Yang Xu	45,243
Steven G. Saunders	36,265		
John J. Stickevers	39,387		
Herbert A. Newborn	42,031		
Jean M. Tibbetts	43,193		
Jeffrey T. Klayman	39,250		
Jay Sandvos	43,900		

Send Correspondence to: John J. Stickevers
 BROMBERG & SUNSTEIN LLP
 125 Summer Street
 Boston, MA 02110

Direct Telephone Calls to: *(name and telephone number)*
 John J. Stickevers at (617) 443-9292

Full name of sole or first inventor Behnam Tabrizi	
Sole or first inventor's signature	Date
Residence 153 Collins Drive, Marlborough, MA 01752	
Citizenship U.S.A.	
Post Office Address Same as residence	

Full name of second inventor, if any	
Second inventor's signature	Date
Residence	
Citizenship	
Post Office Address	